CLAIMS

1. A programmable logic device, comprising at least one address decoder, the or each address decoder comprising:

a first stage, for receiving bits of an address, and for masking out a first group of least significant bits of said address;

a second stage, for comparing a second group of most significant bits of said address with respective comparison bits; and

a third stage, for providing an output when all of the bits in said second group of bits of said address match their respective comparison bits.

2. A programmable logic device as claimed in claim 1, wherein the first stage of the or each address decoder comprises a first number of first AND gates, each for receiving a respective one of said bits of said address, and each for receiving a masking bit determining whether said respective one of said bits of said address is to be masked out.

3. A programmable logic device as claimed in claim 2, wherein the second stage of the or each address decoder comprises a first number of XOR gates, each for receiving an output signal from a respective one of said first AND gates, and each for receiving a respective one of said comparison bits, the comparison bits supplied to the or each address decoder corresponding to the addresses associated with said address decoder.

4. A programmable logic device as claimed in claim 3, wherein the third stage of the or each address decoder comprises a second AND gate having a first number of inputs, each input receiving an inverted output from a respective one of said XOR gates, and said second AND gate providing an output when all of the bits in said second group of bits of said address match their respective comparison bits.

5. A programmable logic device as claimed in claim 1, comprising a plurality of address decoders in hard logic.

6. A programmable logic device as claimed in claim 1, comprising a gate array, and further comprising a plurality of said address decoders at spaced apart locations within said gate array.

7. A programmable logic device as claimed in claim 6, further comprising an embedded processor, said embedded processor being connected to said gate array by means of a bridge.

8. A programmable logic device, comprising:

an embedded processor; and

a field programmable gate array, comprising programmable logic elements,

wherein the field programmable gate array can be used to implement a bus structure and a plurality of slave devices, and the embedded processor can be used as a bus master connected to the bus structure, and

wherein the field programmable gate array further comprises a plurality of address decoders, implemented in hard logic at spaced apart locations within said gate array, such that each of said plurality of slave devices can be connected to a respective one of said plurality of address decoders.

9. A programmable logic device as claimed in claim 8, wherein each address decoder comprises:

a first stage, for receiving bits of an address from said bus master, and for masking out a first group of least significant bits of said address;

a second stage, for comparing a second group of most significant bits of said address with respective comparison bits; and

a third stage, for enabling data, associated with said address from said bus master, to be acted upon in the slave device associated with said address decoder, when all of the bits in said second group of bits of said address match their respective comparison bits.

10. A programmable logic device as claimed in claim 9, further comprising a configuration memory for supplying configuration data to said device, wherein the configuration memory is adapted to supply respective configuration data to each of said address decoders as said respective comparison bits.

11. A programmable logic device as claimed in claim 10, wherein the configuration memory is adapted to supply respective configuration data to each of said address decoders as said respective comparison bits, the respective configuration data

supplied to each address decoder corresponding to the addresses associated with said address decoder.

12. A programmable logic device as claimed in claim 9, wherein the first stage of the or each address decoder comprises a first number of first AND gates, each for receiving a respective one of said bits of said address, and each for receiving a masking bit determining whether said respective one of said bits of said address is to be masked out.

13. A programmable logic device as claimed in claim 12, wherein the second stage of the or each address decoder comprises a first number of XOR gates, each for receiving an output signal from a respective one of said first AND gates, and each for receiving a respective one of said comparison bits, the comparison bits supplied to the or each address decoder corresponding to the addresses associated with said address decoder.

14. A programmable logic device as claimed in claim 13, wherein the third stage of the or each address decoder comprises a second AND gate having a first number of inputs, each input receiving an inverted output from a respective one of said XOR gates, and said second AND gate providing an output when all of the bits in said second group of bits of said address match their respective comparison bits.

15. In a programmable logic device, a method of decoding a received address, comprising:

receiving bits of an address, and masking out a first group of least significant bits of said address;

comparing a second group of most significant bits of said address with respective comparison bits; and

providing an output when all of the bits in said second group of bits of said address match their respective comparison bits.

16. A method as claimed in claim 15, comprising applying received bits of said address to respective first inputs of respective first AND gates, applying respective masking bits to respective second inputs of said respective first AND gates, and masking out received bits of said address which do not match their respective masking bits.

17. A method as claimed in claim 16, comprising applying the outputs of said respective first AND gates to respective first inputs of respective XOR gates, and applying respective comparison bits to respective second inputs of said respective XOR gates, the comparison bits supplied to the or each address decoder corresponding to the addresses associated with said address decoder.

18. A method as claimed in claim 17, comprising applying inverted output bits from said XOR gates to respective inputs of a second AND gate, said second AND gate providing an output when all of the bits in said second group of bits of said address match their respective comparison bits.